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LAYALI RASHID

Research Interests

Computer architecture; reliability and performance. Hardware faults avoidance and tolerance. Performance characterizations and optimizations.

Education

- Ph.D., Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, British Columbia, Canada.
  - Defended successfully on Jan, 2013.
  - Advisers are Karthik Pattabiraman and Sathish Gopalakrishnan.
  - Committee members are Steve Wilton and Alan Hu.
- M.Sc., Department of Electrical and Computer Engineering, University of Calgary, Calgary, Alberta, Canada.
  - Graduated in 2007.
  - Adviser was Wessam Hassanein.
  - GPA is 4/4.
- B.Sc., Department of Computer Engineering, An-Najah National University, Nablus, Palestine. 2005.
  - GPA is 3.3/4.
- Study Abroad, American University in Cairo, Egypt
  - Spring 2004 and winter 2005.

Selected Projects

- **Modeling ARMv8 architecture:** Worked with a team of twenty engineers on toolkits and simulators for ARMv8 architecture. My tasks include building testing infrastructure and debugging hundreds of tests. Tests that I have worked on examine the virtualization layer, security layer, memory hierarchy, floating-point instructions and vector instructions. Further, I conducted characterization studies on cycle-accurate simulators to help the micro-architecture designer build RTL simulator.
- **Cloud-level profiling**: Built a prototype of a cloud-level profiler. My prototype can generate accurate profiles with very low overhead across hundreds of thousands of machines. It supports a wide variety of performance counters and reports. It can be configured to run autonomously or manually. (Internship work)
- **Tolerating hardware-intermittent errors**: My dissertation focus is on mitigating the impact of intermittent hardware errors that affect processors. (Ph.D. work)
  - Modeled the impact of intermittent hardware faults on programs through fault injection experiments in a cycle-accurate Alpha simulator.
  - Studied the impact of different recovery scenarios on the processor performance and reliability through Stochastic Activity Networks.
  - Built a software-based diagnosis technique to isolate the error-prone micro-architectural unit and evaluate my technique through fault injection experiments.
- **Parallelizing database operations:** Built multithreaded data management operations that took advantage of Simultaneous Multithreading and Chip Multiprocessor architectures. The proposed operations provided better load balancing across cores and improved hardware resources utilization. The database operations were the hash join, the sort and the index. (M.Sc. work)
- **Signal generator:** Designed and implemented hardware signal generator that created sine, triangle and square signals and white noise with user-specified parameters (e.g. amplitude and frequency) using microcontrollers with the help of MPLAB 5.20 and Cadence OrCAD Capture 9.2. (B.Sc. work)
- **Firewall:** Programmed a firewall application using network programming skills and Visual C++.Net. (B.Sc. work.)
- **Compiler:** Built a simple compiler using C++. (B.Sc. work)

Skills

- **Teaching skills:** worked as a teaching assistant for C programming language for first-year students for nine courses. Also worked as a teaching assistant for a computer architecture basics course for last-year students. During my work I gave tutorials, supervised laboratories, held office hours, graded exams and homework.
- **Programming languages:** C, C++, C#, Python, Java and assembly (MIPS, Alpha and ARM).
- **Parallel programming skills** with OpenMP, MPI and OpenCL.

- **Parallel architectures:** multithreading, multi/many cores and heterogeneous cores (CPUs and GPGPUs).
- **Web services:** experience with Microsoft Visual Studio 2010 Professional, .NET 4.0 and Windows Communication Foundation (WCF).
- **Performance analysis:** cycle-accurate simulators (SimpleScalar), hardware performance counters, Windows Performance Analyzer and Intel VTune Performance Analyzer.
- **Hardware reliability**: detection, diagnosis and recovery from transient, intermittent and permanent hardware errors.
- **Modeling**: Matlab and Möbius Tool.
- **Operating systems:** experience with Linux Ubuntu and Microsoft Windows.

Selected Publications

- **L. Rashid**, K. Pattabiraman, and S. Gopalakrishnan. "Characterizing the Impact of Intermittent Hardware Faults on Programs". Submitted. (Journal paper, PhD work)
- **L. Rashid**, K. Pattabiraman, and S. Gopalakrishnan. "DIEBA: Diagnosing Intermittent Errors by Backtracing Application Failures". Submitted. (Journal paper, PhD Work)
- **L. Rashid**, K. Pattabiraman, and S. Gopalakrishnan. "Intermittent Hardware Errors Recovery: Modeling and Evaluation". International Conference on Quantitative Evaluation of SysTems. 2012. (PhD Work)
- **L. Rashid**, K. Pattabiraman, and S. Gopalakrishnan. "DIEBA: Diagnosing Intermittent Errors by Backtracing Application Failures". IEEE Workshop on Silicon Errors in Logic - System Effects. 2012. (PhD Work)
- **L. Rashid**, K. Pattabiraman and S. Gopalakrishnan. "Modeling the Propagation of Intermittent Hardware Faults in Programs". IEEE Pacific Rim International Symposium on Dependable Computing. 2010. (PhD Work)
- **L. Rashid**, K. Pattabiraman and S. Gopalakrishnan. "Towards Understanding the Effects of Intermittent Hardware Faults on Programs". Workshop on Dependable and Secure Nanocomputing, in conjunction with the International Conference on Dependable Systems and Networks. 2010. (PhD Work)
- **L. Rashid**, K. Pattabiraman and S. Gopalakrishnan. "Formal Diagnosis of Hardware Transient Errors in Programs". IEEE Workshop on Silicon Errors in Logic- System Effects. 2010. (PhD Work)
- **L. Rashid**, W.M. Hassanein, and M.A. Hammad. "Analyzing and Enhancing the Parallel Sort Operation on Multithreaded Architectures". The Journal of Supercomputing. 2009. (M.Sc. Work)
- W.M. Hassanein, **L. Rashid**, and M.A. Hammad. "Analyzing the Effects of Hyper-threading on the Performance of Data Management Systems". International Journal of Parallel Programming. 2008. (M.Sc. Work)
- **L. Rashid**, W.M. Hassanein, and M.A. Hammad. "Exploiting Multithreaded Architectures to Improve the Hash Join Operation". Workshop on Memory Performance: Dealing with Applications, Systems and Architecture, held in conjunction with the International Conference on Parallel Architectures and Compilation Techniques. 2008. (M.Sc. Work)
- W.M. Hassanein, M.A. Hammad, and **L. Rashid**. "Characterizing the Performance of Data Management Systems on Hyper-Threaded Architectures". International Symposium on Computer Architecture and High Performance Computing. 2006. (M.Sc. Work)

Work Experience

- CPU Performance Modeling Engineer in Qualcomm Technologies Inc. March, 2012 – Current.
- Research Intern in Microsoft Research, Redmond, WA, USA. Summer, 2011.
- Teaching and Research Assistant, University of British Columbia, Vancouver, BC, Canada. 2007-2012.
- Teaching and Research Assistant, University of Calgary, Calgary, AB, Canada. 2005-2007.
- Undergraduate Intern at the Palestinian Telecommunication Group, Palestine. Summer, 2004.

Awards and Honors

- Four Year Fellowship. University of British Columbia, 2009-2011.
- Alexander Graham Bell Canada Graduate Scholarship, 2009-2011.
- Graduate Entrance Scholarship. University of British Columbia, 2007.
- Queen Elizabeth II Graduate Scholarship. Calgary, Alberta, 2007.
- Travel Awards:
    - International Conference on Dependable Systems and Networks, 2012.
    - ASPLOS Google Conference Travel Award, 2011.
    - USENIX Symposium on Operating Systems Design and Implementation, 2010
    - International Conference on Dependable Systems and Networks, 2010.
    - International Conference on Parallel Architectures and Compilation Techniques, 2008.
    - University of Calgary (Travel award to the 20th Canadian Conference on Electrical and Computer Engineering in Vancouver), 2007.

- Alberta Graduate Student Scholarship, 2006.
- American University in Cairo Scholarship for International Students. Egypt, 2004-2005.
- Top 10% undergraduate students at the Computer Engineering Department. An-Najah National University. Palestine, 2002-2005.
- Top 5% undergraduate students at the Computer Engineering Department. An-Najah National University. Palestine, 2000-2001.